We claim

1. A global positioning system (GPS) receiver, comprising:

a converter for converting received GPS signals to in-phase (I) and quadrature-phase (Q) digital signals;

a correlator for generating expected codes and correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values for a tap;

a filter for filtering the sampled I values and sampled Q values to modified I values and modified Q values, and for summing the modified I values and modified Q values to output variation data;

a memory for storing the variation data;

a domain transformer for performing domain transform on the variation data to output a transformed value; and

a comparator for comparing the transformed value to a threshold value for determining the presence of a peak at the tap.

2. The receiver of claim 1, wherein the sampled I values and sampled Q values are modified by assigning a positive value to the sampled I value or sampled Q value when a present sample I value or Q value has a different sign from the immediately prior sample I value or sample Q value.

3. The receiver of claim 1, wherein the modified I values and modified Q

values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

4. The receiver of claim 3, wherein the fractional reduction is one half.

5. The receiver of claim 1, wherein the filter includes a pair of delay elements and a pair of single bit comparators, wherein the delay elements delay a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and the single bit comparators compare a sign of the present sampled Q value with the prior sign value to provide a positive output if the present and the prior sign values are different.

6. The receiver of claim 5, wherein the filter further includes an adder for performing the summing operation on the modified I value with the modified Q value, including the sign bits.

7. The receiver of claim 1, wherein the domain transformer is a Fast Fourier Transformer.

8. The receiver of claim 1, wherein the memory further stores the sampled I and Q values of the tap identified as having a peak.

9. The receiver of claim 1, wherein the memory is one of a SRAM and a DRAM.

10. A global positioning system (GPS) receiver, comprising:

a converter for converting received GPS signals of a tap to in-phase (I) and quadrature-phase (Q) digital signals;

a correlator for correlating the I and Q digital signals with expected codes to output sampled I values and sampled Q values, each of the sampled I values and sampled Q values having a sign bit for signifying direction;

a filter for filtering at least the sign bits of the sampled I values and sampled Q values and determining whether a potential peak exists at the tap based on the number of change in directions in the sign bits of the sampled I values and sampled Q values;

a domain transformer for performing domain transform on data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak and outputting a transformed value; and

a comparator for comparing the transformed value to a threshold value for determining the presence of a peak at the tap.

11. The receiver of claim 10, further including a memory for storing the data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak.

12. The receiver of claim 11, wherein the memory is one of a SRAM and a DRAM.

13. The receiver of claim 10, wherein the data is derived from the sampled I values and sampled Q values by adding sign-modified I values to sign-modified Q values.

14. The receiver of claim 10, wherein the sampled I values and sampled Q values are filtered by assigning a positive value to the sampled I value or sampled Q value when a present sample I value or Q value has a different sign from the immediately prior sample I value or sample Q value.

15. The receiver of claim 14, wherein the filtered I values and filtered Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

16. The receiver of claim 10, wherein the filter includes a pair of delay elements and a pair of single bit comparators, wherein the delay elements delay a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and the single bit comparators compare a sign of the present sampled Q value with the prior sign value to provide a positive output if the present and the prior sign values are different.

17. A method for processing global positioning system (GPS) signals for determining position, comprising:

receiving GPS signals from one or more satellites;

converting the received GPS signals to in-phase (I) and quadrature-phase (Q) digital signals of a tap;

generating expected codes and correlating the I and Q digital signals with the expected codes to output sampled I values and sampled Q values;

filtering the sampled I values and sampled Q values to modified I values and modified Q values, and summing the modified I values and modified Q values to output variation data;

storing in memory the variation data;

performing domain transform on the variation data to output a transformed value; and

comparing the transformed value to a threshold value for determining the presence of a peak at the tap.

18. The method of claim 17, wherein the sampled I values and sampled Q values are modified by assigning a negative value to the sampled I value or sampled Q value when a present sampled I value or Q value has a different sign from the immediately prior sampled I value or sampled Q value.

19. The method of claim 17, wherein the modified I values and modified Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

20. The method of claim 19, wherein the fractional reduction is one half.

21. The method of claim 17, wherein the step of filtering includes delaying a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and comparing a sign of the present sampled Q value with the prior sign value to provide a negative output if the present and the prior sign values are different.

22. The receiver of claim 21, wherein the step of filtering further includes summing the modified I value with the modified Q value, including the sign bits.

23. The method of claim 17, wherein the domain transform is Fast Fourier Transform.

24. The method of claim 17, further including storing in the memory the sampled I and Q values of the tap identified as having a peak and discarding sampled I and Q values of other taps.

25. A method for processing global positioning system (GPS) signals, comprising:

converting received GPS signals of a tap to in-phase (I) and quadrature-phase (Q) digital signals;

correlating the I and Q digital signals with expected codes to output sampled I values and sampled Q values, each of the sampled I values and sampled Q values having a sign bit for signifying direction;

filtering at least the sign bits of the sampled I values and sampled Q values and determining whether a potential peak exists at the tap based on the number of change in directions in the sign bits of the sampled I values and sampled Q values;

performing domain transform on data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak and outputting a transformed value; and

comparing the transformed value to a threshold value for determining the presence of a peak at the tap.

26. The method of claim 25, further including storing in a memory the data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak.

27. The method of claim 26, wherein the memory is one of a SRAM and a DRAM.

28. The method of claim 25, wherein the data is derived from the sampled I values and sampled Q values by adding sign-modified I values to sign-modified Q values.

29. The method of claim 25, wherein the sampled I values and sampled Q values are filtered by assigning a positive value to the sampled I value or sampled Q value when a present sample I value or Q value has a different sign from the immediately prior sample I value or sample Q value.

30. The method of claim 25, wherein the filtered I values and filtered Q values are fractional reductions of respective sampled I values and sampled Q values, the fractional reduction being the same for both the sampled I values and the sampled Q values.

31. The method of claim 25, wherein the step of filtering includes delaying a sign bit of the sampled I value and the sampled Q value to output a prior sign value, and comparing a sign of the present sampled Q value with the prior sign value to provide a positive output if the present and the prior sign values are different.

32. A stored program device having stored codes executable by a processor to perform method steps for processing GPS signals, the method comprising:

correlating I and Q digital signals with expected codes to output sampled I values and sampled Q values, each of the sampled I values and sampled Q values having a sign bit for signifying direction;

filtering at least the sign bits of the sampled I values and sampled Q values and determining whether a potential peak exists at the tap based on the number of change in directions in the sign bits of the sampled I values and sampled Q values;

performing domain transform on data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak and outputting a transformed value; and

comparing the transformed value to a threshold value for determining the presence of a peak at the tap.

33. The method of claim 32, further including storing in a memory the data derived from the sampled I values and sampled Q values of the tap determined to have a potential peak.

34. The method of claim 33, wherein the memory is one of a SRAM and a DRAM.

35. The method of claim 32, wherein the data is derived from the sampled I values and sampled Q values by adding sign-modified I values to sign-modified Q values.

36. The stored program device of claim 32, wherein the stored program device is one of a flash memory or ROM.